REMARKS

This application has been revised and the following remarks are submitted in light of the Office Action mailed July 27, 2005 and the Examiner Interview conducted on October 18, 2005. Applicants appreciate the courtesies extended by the Examiner during the Examiner Interview. Agreement appears to have been reached during the Examiner Interview, and this detailed response is submitted in accordance with the discussions during the Examiner Interview. Claim 1-16 are presented for examination. Claim 1 has been amended.

The claim amendments presented herein are fully supported by the specification as originally filed. Claim 1 as amended is supported by the specification at paragraphs [0014] and [0015]. In addition, a new paragraph has been added to the specification to denote Figure 3. No new matter has been added.

Objection to the Drawings under 37 C.F.R. 1.83a

The drawings are objected to because the drawings are found to lack "a plurality of integrated circuit chips fabricated on a substrate" as recited in claim 1, "a plurality of layers of said at least one second dielectric material" as recited in claim 15. Figure 1 submitted as a replacement sheet filed on February 4, 2005 depicts a plurality of integrated circuit chips fabricated on a substrate. Figure 2 has been amended to show more than integrated circuit chips fabricated on a substrate. A new Figure 3 has been submitted that illustrates more than one layer of the second dielectric material as recited in claim 15. Replacement drawing sheets 1, 2, and 3 are submitted herewith. Applicants therefore submit that this objection to the drawings has been overcome.

Rejection of Claims 1-16 under 35 U.S.C. 112, second paragraph

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph as being indefinite. Applicants respectfully traverse this rejection.

In Claim 1, the features "a substrate", "integrated circuits chips;" and "of said integrated circuits" are found to be unclear and confusing. As currently amended, Claim 1 requires "integrated circuit chips." Figure 2 has been amended to show more

than one integrated circuit chip 11 on the substrate 10. Applicants therefore submit that Claim 1, when read in the light of the specification and drawings, is not indefinite.

In Claim 15, the feature "said semiconductor wafer comprises a plurality of layers of said at least one second dielectric material." Figure 3 has been added and reference thereto added to the specification that shows the second dielectric material 17 comprised of more than one layer. Applicants therefore submit that Claim 15, when read in light of the specification and drawings, is not indefinite.

In Claim 16, the feature "at least one of said layers of second dielectric material is SiO2 and at least one of said layers of second dielectric material is SiNx." Figure 3 demonstrates the appropriate shading for both types of material. Applicants therefore submit that Claim 16, when read in light of the specification and drawings, is not indefinite.

Rejection of Claims 1-12 under 35 U.S.C. 102(e) over Massingill

Claims 1-12 are rejected under 35 U.S.C. 102(e) over U.S. Patent No. 6,882,045 to Massingill. Applicants respectfully traverse this rejection.

Claim 1 is directed to a semiconductor wafer comprising a substrate, a plurality of integrated circuit chips fabricated on the substrate, a dicing channel disposed between the integrated circuit chips, a layer of first dielectric material disposed on the integrated circuit chips, and a second dielectric material disposed on the first dielectric material, wherein the first dielectric material has a G_c value of at least about 10 times greater than the second dielectric material. Thus, it is a feature of the invention that two distinct dielectric materials are disposed on the integrated circuit chips and it is a further feature of the invention that the first dielectric material has a critical strain energy release rate 10 times greater than the second dielectric material.

The claimed invention solves the problem of probing, dicing, and packaging chips containing low-k insulators. More specifically, the claimed invention prevents fracture, chipping, or cracking of the low-k insulator. The claimed invention accomplishes such benefit through the use of two dielectric layers disposed over the integrated circuit chip. Each dielectric layer has distinct material properties. More

specifically, the first dielectric material has a critical strain energy release rate, i.e. G_c, 10 times greater than the second dielectric material. The benefit of the claimed invention is the interdependency of two dissimilar dielectric materials with distinctly different material properties. The first dielectric material absorbs mechanical stresses while the second dielectric material hermetically seals the chip, prior to dicing. (Specification [0015])

Massingill is directed to a semiconductor chip with capacitor structures embedded therein. The integrated circuit chip 442 as shown in Figure 76 has capacitor structures of which aperture 422 forms a part. Massingill fails to disclose a first and second dielectric material disposed over the integrated circuit chip 442. Moreover, Massingill fails to disclose a critical strain energy release ratio that differs between a first and second dielectric material disposed over the integrated circuit chip 442. Massingill also fails to disclose a dicing channel. Reference 490 denotes a via. Since Massingill fails to disclose each and every element of the claimed invention, Applicants respectfully submit that Claim 1 is not anticipated by Massingill. Claims 2-16, which depend from claim 1, also are not anticipated by Massingill. Applicants therefore request withdrawal of this rejection.

Rejection of Claims 1-8 and 10-16 under 35 USC 103 over Farnworth

Claims 1-8 and 10-16 are rejected under 35 U.S.C. 103 over U.S. Patent No. 5,786,632 to Farnworth. Applicants respectfully traverse this rejection.

As discussed previously, it is a feature of the invention that two distinct dielectric materials are disposed on the integrated circuit chips and it is a further feature of the invention that the first dielectric material has a critical strain energy release rate 10 times greater than the second dielectric material.

Farnworth is directed to semiconductor packaging. A protective layer 36 covers the face of a die 30. The protective layer 36 extends over the exposed vertical edge of the circuitry 48 but does not go over the edge of the die 30 substantially as shown in FIG. 3. (Farnworth, col. 4, lines 23-26). Farnworth fails to disclose two distinct dielectric materials disposed on the integrated circuit chips. Farnworth further fails to disclose

that the first dielectric material has a critical strain energy release rate at least ten times greater than the second dielectric material.

Farnworth also fails to suggest these features of the present invention. Farnworth is directed to a protective layer 36 that protects the face of the die 30 and that functions as a guide surface for guiding the connectors 90 on a holder 70 into electrical contact with contact pads 34 (Farnworth, col. 5, lines 3-20). Farnworth fails to recognize the importance of a first dielectric material that absorbs mechanical stresses of an integrated circuit chip and a second dielectric material that hermetically seals the integrated circuit chip. Accordingly, Applicants respectfully submit that Claim 1 is patentable over Farnworth. Claims 2-8 and 10-16, which depend from Claim 1, are also patentable over Farnworth, by virtue of their dependence on a patentable base claim. Applicants respectfully request withdrawal of this rejection.

Rejection of Claims 13-16 under 35 U.S.C. 103 (a) over Massingill

Claims 13-16 are rejected under 35 U.S.C. 103(a) over Massingill. Applicants respectfully traverse this rejection.

Claims 13-16 depend from Claim 1. As discussed previously, it is a feature of the present invention that two distinct dielectric materials are disposed on the integrated circuit chips and it is a further feature of the invention that the first dielectric material has a critical strain energy release rate 10 times greater than the second dielectric material. Applicants respectfully submit that these features are neither disclosed nor suggested by Massingill.

Massingill fails to disclose a first and second dielectric material disposed over the integrated circuit chip 442. Moreover, Massingill fails to disclose a critical strain energy release rate ratio that differs between a first and second dielectric material disposed over the integrated circuit chip 442.

Accordingly, Applicants respectfully submit that Claim 1 is patentable over Massingill. Claims 13-16, which depend from Claim 1, also are patentable over Massingill. It is a feature of claim 13 that a plurality of conductors are embedded in the first and second dielectric material. Massingill fails to disclose or even suggest a

plurality of conductors embedded in a first dielectric material. It is a feature of Claim 14, which depends from claim 13, that these conductors are jogged. The conductors 14, as shown in Figure 1 of the specification, have a jogged shape. Massingill further fails to disclose or suggest conductors with a jogged shape. It is a feature of claim 15 that the second dielectric material comprises a plurality of layers. Massingill fails to disclose or suggest a second dielectric material with a plurality of layers. Claim 16, which depends from claim 15, is also patentable over Massingill. For these additional reasons, Applicants therefore request withdrawal of the rejection of these claims.

Rejection of Claim 9 under 35 U.S.C. 103(a) over Farnworth in view of Sun

Claim 9 is rejected under 35 U.S.C. 103(a) over Farnworth in view of Sun. Applicants respectfully traverse this rejection.

Claim 9 depends from Claim 1. As discussed previously, it is a feature of the present invention that two distinct dielectric materials are disposed on the integrated circuit chips and it is a further feature of the invention that the first dielectric material has a critical strain energy release rate 10 times greater than the second dielectric material. Applicants respectfully submit that these features are neither disclosed nor suggested by Farnworth.

Sun fails to compensate for the deficiencies of Farnworth. Sun is directed to a method of removing a passivation material overlying a memory link. Sun fails to disclose or suggest two dielectric materials disposed on the integrated circuit chips with distinct critical strain energy release rates. Accordingly, Applicants respectfully submit that Claim 1 is patentable over Farnworth in view of Sun. Claim 9, which depends from Claim 1, is also patentable over Farnworth in view of Sun. Applicants therefore respectfully request withdrawal of this rejection.

It is respectfully submitted that the present application is in condition for allowance.

Reconsideration and allowance of pending claims is respectfully requested.

Conclusion

Applicants have properly traversed each of the grounds for rejection in the Office Action, and therefore submit that the present application is now in condition for allowance. If the Examiner has any questions or believes further discussion will aid examination and advance prosecution of the application, a telephone call to the undersigned is invited.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, the Commissioner is authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully Submitted,

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